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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/547,167	04/11/00	KENNEDY J	30-4885 (478

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EXAMINER	
NOVACEK,C	
ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 08/24/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/547,167	KENNEDY ET AL.	
	Examiner	Art Unit	
	Christy L. Novacek	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 April 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This Office Action is in response to the communication filed April 11, 2000.

Specification

1. The disclosure is objected to because of the following informalities: On page 5, line 20, "Figures 2a-2g" should be changed to "Figures 2a-2h".

Appropriate correction is required.

2. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required:

The specification does not provide support for the limitation of polymeric material obtained from phenyl-ethynylated aromatic monomers and oligomers, as stated in lines 4-5 of claims 4 and 5. See page 7, lines 1-8 of the specification.

The specification does not disclose what the second organic intermetal dielectric layer is made of. Thus, it fails to provide support for claims 11 and 32. See page 7, lines 17-20 of the specification.

The specification does not explicitly provide support for the limitation of forming the hardmask layer of "mixtures" of silicon oxide and silicon oxynitride, as stated in claims 7, 12, 16, 28, and 33. See page 7, lines 21-23 of the specification.

The specification does not explicitly provide support for the limitation of forming the etch stop layer from "silicon nitride" or "mixtures" of silicon nitride and silicon oxide, as stated in claims 10 and 31. See page 7, lines 13-15.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 4-7, 10-12, 16, 28, and 31-33 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

In reference to claims 4-7, the specification does not provide support for the limitation of polymeric material obtained from phenyl-ethynylated aromatic monomers and oligomers, as stated in lines 4-5 of claims 4 and 5. See page 7, lines 1-8 of the specification. Claims 6-7 are rejected for their dependence upon claims 4-5.

In reference to claims 10 and 31, the specification does not explicitly provide support for the limitation of forming the etch stop layer from "silicon nitride" or "mixtures" of silicon nitride and silicon oxide, as stated in claims 10 and 31. See page 7, lines 13-15.

In reference to claims 11 and 32, the specification does not disclose what the second organic intermetal dielectric layer is made of. Thus, it fails to provide support for claims 11 and 32. See page 7, lines 17-20 of the specification.

In reference to claims 7, 12, 16, 28, and 33, the specification does not explicitly provide support for the limitation of forming the hardmask layer of "mixtures" of silicon oxide and silicon oxynitride, as stated in claims 7, 12, 16, 28, and 33. See page 7, lines 21-23 of the specification.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 22, 25, 35 and 37 are rejected under 35 U.S.C. 102(b) as being anticipated by Avanzino et al. (US 5,795,823).

In reference to claim 22, Avanzino ('823) discloses depositing a stack comprising a first intermetal dielectric layer which may be organic (52) onto a substrate (51) (col. 8, ln. 51-53). A line opening (55) is formed in the stack and a sacrificial inorganic dielectric (70) is deposited into the opening, such that the opening is substantially filled (Fig. 5g-5r; col. 60-64). A via opening (58) is formed in the stack and inorganic dielectric and the line and via openings are filled with conducting material (80) (col. 8, ln. 11-14).

In reference to claim 25, the organic dielectric layer may be a polyimide (col. 8, ln. 51-52).

In reference to claim 35, the conducting material is an aluminum-copper alloy (col. 8, ln. 12-14).

In reference to claim 37, the substrate is disclosed as being a semiconductor device or other interconnect layers (col. 8, ln. 45-51).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-6, 8-11, 13-15 and 17-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art in view of Avanzino et al. (US 5,795,823) and Pellerin et al.

In reference to claim 1, the admitted prior art discloses depositing a stack comprising a first organic intermetal dielectric layer (102) onto a substrate (100). A via opening (104) is formed in the stack and a sacrificial dielectric (105) is deposited into the opening, such that the opening is substantially filled. A line opening (107) aligned with the via opening is formed in the stack and inorganic dielectric and the line and via openings are filled with conducting material (Fig. 1a-1d; pg. 3, ln. 7-pg. 4, ln. 12). The admitted prior art discloses using an organic material to comprise the sacrificial layer but also discloses that by using organic material to comprise sacrificial layer, this process typically results in degradation of the critical dimensions of the interconnect pattern (pg. 3, ln. 25-29). Like the admitted prior art, Avanzino ('823) also discloses a process of using a sacrificial layer to etch a line/via interconnect pattern. However, Avanzino teaches that it is advantageous to use a sacrificial layer which can be etched selectively to the intermetal dielectric in order to improve the accuracy of the etch, and thus improve the definition of the interconnect structure (col. 2, ln. 2-5; col. 5, ln. 4-16). Avanzino discloses that the intermetal dielectric (52) may be organic and also discloses that the sacrificial dielectric (70) may be inorganic. Like the admitted prior art and Avanzino, Pellerin also discloses a process of

using a sacrificial layer (24) to etch a line/via interconnect pattern. And like Avanzino, Pellerin also discloses that it is advantageous to use a sacrificial layer which can be etched selectively to the intermetal dielectric (16) (Fig. 1-5; Abstract; col. 4, ln. 65-col. 5, ln. 1). Specifically, Pellerin recommends that when using an organic intermetal dielectric layer, the sacrificial dielectric should comprise an inorganic, silicon based material (col. 4, ln. 65-col. 5, ln. 1). At the time of the invention, it would have been obvious to one of ordinary skill in the art to replace the sacrificial layer of the admitted prior art with a material that has a high etching selectively with respect to the intermetal organic dielectric layer as is taught by Avanzino. Furthermore, in light of the teachings of Pellerin, it would have been obvious to one of ordinary skill in the art to form the sacrificial dielectric layer from an inorganic material in order to provide the high degree of etching selectivity required for precise definition of the interconnect structure.

In reference to claims 2 and 3, Avanzino et al. disclose that a number of insulating materials may be used in accordance with their invention (col. 8, ln. 39-45). Pellerin specifically discloses that the sacrificial inorganic dielectric layer may be made of a silicate, a silsesquioxane, a silica gel, or methyl silsesquioxane (col. 4, ln. 10-15; col. 4, ln. 61-col. 5, ln. 1). These compounds would inherently have the ratio of H, Si, O and R that are stated in claim 2 of the present application. At the time of the invention, it would have been obvious to one of ordinary skill in the art to use one of the inorganic materials such as the methyl siloxane disclosed by Pellerin to comprise the sacrificial dielectric because Avanzino discloses that any number of insulating materials that are known in the art may be used to comprise the sacrificial layer.

In reference to claim 4, the admitted prior art does not disclose what material the organic intermetal dielectric is made from. Avanzino discloses that organic intermetal dielectrics

comprising polyimides are known in the art (col. 8, ln. 51-53). Pellerin discloses comprising the organic intermetal dielectric layer of a material such as a poly arylene ether, an oligomeric hydrocarbon, a poly(paraxylylene), a poly(tetrafluoroethylene), a polyimide, or a divinyl siloxane (col. 4, ln. 2-11).

In reference to claim 5, the admitted prior art discloses forming a diffusion barrier layer (101) between the substrate (100) and the organic intermetal dielectric layer (102) and also forming a hardmask layer (103) on the organic intermetal layer (pg. 3, ln. 7-9).

In reference to claim 6, the admitted prior art does not disclose what material comprises the diffusion barrier layer. However, Avanzino, which also discloses forming a barrier layer, teaches comprising the layer of silicon nitride (col. 6, ln. 29-35). In fact, such barrier layers used in interconnect structures are conventionally formed from silicon nitride. At the time of the invention, it would have been obvious to one of ordinary skill in the art to form the barrier layer of the admitted prior art from silicon nitride because it is known and conventional in the art to form such layers from silicon nitride.

In reference to claim 8, the admitted prior art discloses forming a diffusion barrier layer (101) between the substrate (100) and the organic intermetal dielectric layer (102) and also forming a hardmask layer (103) on the organic intermetal layer (pg. 3, ln. 7-9). Avanzino discloses that, as an alternative to forming one organic intermetal dielectric layer, two organic intermetal dielectric layers may be used with the two layers being separated by an etch stop layer in order to more precisely etch separate line and via portions (col. 6, ln. 12-20). At the time of the invention, it would have been obvious to one of ordinary skill in the art to substitute two organic layers with an etch stop layer in between as taught by Avanzino for the single organic

layer disclosed by the admitted prior art, in order to obtain more precise etching of the separate line and via portions.

In reference to claim 9, at the time of the invention, it would have been obvious to one of ordinary skill in the art to form the diffusion barrier layer of the admitted prior art of silicon nitride for the reasons stated above in reference to claim 6.

In reference to claim 10, Avanzino discloses forming the etch stop of silicon nitride (col. 6, ln. 31-33).

In reference to claim 11, Avanzino discloses using organic intermetal dielectric layers such as polyimide and also discloses that both the first and second intermetal dielectric layers may be made of the same material (col. 8, ln. 51-52; col. 6, ln. 1-28).

In reference to claim 13, the admitted prior art discloses using only one organic intermetal dielectric layer. Avanzino discloses that, as an alternative to using only one intermetal dielectric layer, two intermetal layers may be used. The bottom intermetal layer (52a") is made of a material that is different than the second intermetal layer (52b") so that the etching selectivity of the two layers with respect to each other can be used to precisely etch separate line and via portions (Fig. 4a"; col. 6, ln. 20-28). Avanzino discloses that intermetal dielectric layers may be made of either organic or inorganic materials, but does not specifically disclose using a bottom inorganic layer with an overlying organic layer. Avanzino discloses that any number of insulating materials that are known in the art may be substituted for the materials specifically disclosed in their patent (col. 8, ln. 39-45). Pellerin discloses that when forming a line/via interconnect structure, it is advantageous to use two different intermetal layers. The bottom intermetal layer (16) is used to form the via portion of the interconnect and may be made of an

inorganic material. The top intermetal layer (24) is used to form the line portion of the interconnect and may be made of an organic material (col. 4, ln. 61-col. 5, ln. 1). The two intermetal layers of different etching selectivities provide precise etching of the separate line and via portions. At the time of the invention, it would have been obvious to one of ordinary skill in the art to replace the single intermetal layer of the admitted prior art with two intermetal layers that have a high etching selectively with respect to each other (such that the bottom layer may comprise an inorganic material while the top layer comprises an organic layer) in order to provide the high degree of etching selectivity required for precise definition of the separate line and via portions of each interconnect structure.

In reference to claim 14, at the time of the invention, it would have been obvious to one of ordinary skill in the art to form the diffusion barrier layer of the admitted prior art of silicon nitride for the reasons stated above in reference to claim 6.

In reference to claim 15, Avanzino et al. disclose that a number of insulating materials may be used in accordance with their invention (col. 8, ln. 39-45). Pellerin specifically discloses that the inorganic intermetal dielectric layer may be made of a silicate, a silsesquioxane, a silica gel, or methyl silsesquioxane (col. 4, ln. 10-15; col. 4, ln. 61-col. 5, ln. 1). These compounds would inherently have the ratio of H, Si, O and R that are stated in claim 2 of the present application. At the time of the invention, it would have been obvious to one of ordinary skill in the art to use one of the inorganic materials disclosed by Pellerin to comprise the bottom layer of the intermetal dielectric because Avanzino discloses that any number of insulating materials that are known in the art may be used to comprise the insulating layers.

In reference to claim 17, the Pellerin discloses that the type etchant used to etch the sacrificial inorganic layer is a matter of design choice that will depend upon the materials selected for the both the first intermetal layer and the sacrificial (col. 5, ln. 21-32). The admitted prior art discloses that a buffered oxide etch can be conducted using *standard* mixture of HF and H_2O. At the time of the invention, it would have been obvious to one of ordinary skill in the art to choose an appropriate etchant such as a buffered oxide etch, as a matter of design choice, based upon the specific type of dielectric layers being utilized.

In reference to claim 18, the admitted prior art does not disclose what the conducting material is comprised of. Avanzino and Pellerin discloses that the conductive interconnect material may be made of a copper or aluminum alloy (col. 4, ln. 59-60 of Pellerin; col. 7, ln. 23-26 of Avanzino). In fact, it is known and conventional in the art to comprise interconnect metallization of aluminum or copper alloys. At the time of the invention, it would have been obvious to one of ordinary skill in the art to form the conducting layer of the admitted prior art from an aluminum or copper alloy because it is known and conventional in the art to form such interconnect metallization from aluminum or copper alloys.

In reference to claim 19, the admitted prior art does not disclose forming a conducting diffusion barrier material in conjunction with the conductive material. Pellerin discloses that a conductive liner comprising tantalum or titanium may be used in conjunction with the conductive material to fill in the via/line metallization portions (col. 5, ln. 56-60). Liners of this type are well known in the art to provide a barrier to diffusion of the bulk conducting interconnect material. At the time of the invention, it would have been obvious to one of ordinary skill in the art to provide a liner to the via/line of the admitted prior art because it is

conventional in the art to do so in order to prevent diffusion of the bulk conducting interconnect material into the surrounding insulative layers.

In reference to claim 20, the admitted prior art does not disclose what the substrate (100) is comprised of. However, Avanzino and Pellerin disclose that typical substrates upon which interconnect metallization layers are built upon include semiconductor wafers, dielectric layers and metal interconnect layers in integrated circuits (col. 8, ln. 45-51 of Avanzino; col. 3, ln. 34-46 of Pellerin). At the time of the invention, it would have been obvious to one of ordinary skill in the art to form the interconnect metallization of the admitted prior art upon a substrate of semiconductor wafers, dielectric layers or metal interconnect layers in integrated circuits because these are all conventional substrates upon which interconnect metallization is formed.

In reference to claim 21, the admitted prior art discloses forming the via and line openings by etching the hardmask layer with a fluorocarbon based plasma and the organic intermetal dielectric layer is etched with an oxygen based plasma (pg. 3, ln. 30-pg. 4, ln. 4).

2. Claims 23-24, 34 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Avanzino et al. (US 5,795,823) as applied to claim 22 above, and further in view of the Pellerin et al. and the admitted prior art.

In reference to claims 23 and 24, Avanzino et al. disclose that a number of insulating materials may be used in accordance with their invention (col. 8, ln. 39-45). Pellerin specifically discloses that the sacrificial inorganic dielectric layer may be made of a silicate, a silsesquioxane, a silica gel, or methyl silsesquioxane (col. 4, ln. 10-15; col. 4, ln. 61-col. 5, ln. 1). These compounds would inherently have the ratio of H, Si, O and R that are stated in claim 2 of the

present application. At the time of the invention, it would have been obvious to one of ordinary skill in the art to use one of the inorganic materials such as the methyl siloxane disclosed by Pellerin to comprise the sacrificial dielectric because Avanzino discloses that any number of insulating materials that are known in the art may be used to comprise the sacrificial layer.

In reference to claim 34, the Pellerin discloses that the type etchant used to etch the sacrificial inorganic layer is a matter of design choice that will depend upon the materials selected for the both the first intermetal layer and the sacrificial (col. 5, ln. 21-32). The admitted prior art discloses that a buffered oxide etch can be conducted using *standard* mixture of HF and H_2O. At the time of the invention, it would have been obvious to one of ordinary skill in the art to choose an appropriate etchant to etch the sacrificial dielectric such as a buffered oxide etch, as a matter of design choice, based upon the specific type of dielectric layers being utilized.

In reference to claim 36, Avanzino does not disclose forming a conducting diffusion barrier material in conjunction with the conductive material. Pellerin discloses that a conductive liner comprising tantalum or titanium may be used in conjunction with the conductive material to fill in the via/line metallization portions (col. 5, ln. 56-60). Liners of this type are well known in the art to provide a barrier to diffusion of the bulk conducting interconnect material. At the time of the invention, it would have been obvious to one of ordinary skill in the art to provide a liner to the via/line of Avanzino because it is conventional in the art to do so in order to prevent diffusion of the bulk conducting interconnect material into the surrounding insulative layers.

3. Claims 26-27, 29-32 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Avanzino et al. (US 5,795,823) in view of the admitted prior art.

In reference to claim 26, Avanzino discloses forming a hardmask layer (53) on the organic intermetal dielectric layer, but does not disclose forming a diffusion barrier layer between the substrate and the intermetal dielectric (col. 6, ln. 5-10). However, Avanzino discloses that their invention is applicable to forming multilevel interconnection layers in addition to forming an interconnect layer on a semiconductor substrate (col. 8, ln. 45-51). The admitted prior art discloses forming a diffusion barrier layer (101) between the substrate (100) and the organic intermetal dielectric layer (102) and also forming a hardmask layer (103) on the organic intermetal layer (pg. 3, ln. 7-9). At the time of the invention, it would have been obvious to one of ordinary skill in the art to form a diffusion barrier layer on the "substrate" of Avanzino in the event that the substrate is a lower interconnect layer. As can be seen by Fig. 3e, 4l and 5r of Avanzino, the top barrier layer on the intermetal dielectric layer would act as a diffusion barrier in the case that the interconnect level in these figures is used as a substrate for subsequently formed interconnect levels.

In reference to claim 27, Avanzino discloses that the barrier layer (53) which will form the diffusion barrier layer of subsequently formed interconnect layers is comprised of silicon nitride (col. 6, ln. 29-35).

In reference to claim 29, Avanzino discloses that, as an alternative to forming one organic intermetal dielectric layer, two organic intermetal dielectric layers may be used with the two layers being separated by an etch stop layer in order to more precisely etch separate line and via portions (col. 6, ln. 12-20). Avanzino does not disclose a diffusion barrier layer between the substrate and the first organic intermetal dielectric layer. However, as stated above in reference to claim 26, it would have been obvious to one of ordinary skill in the art to form a diffusion

barrier layer on the "substrate" of Avanzino in the event that the substrate is a lower interconnect layer.

In reference to claim 30, Avanzino discloses that the barrier layer (53) which will form the diffusion barrier layer of subsequently formed interconnect layers is comprised of silicon nitride (col. 6, ln. 29-35).

In reference to claim 31, Avanzino discloses forming the etch stop of silicon nitride (col. 6, ln. 31-33).

In reference to claim 32, Avanzino discloses using organic intermetal dielectric layers such as polyimide and also discloses that both the first and second intermetal dielectric layers may be made of the same material (col. 8, ln. 51-52; col. 6, ln. 1-28).

In reference to claim 38, Avanzino discloses etching the intermetal dielectric layer using a fluorocarbon plasma (when the dielectric comprises an inorganic material) but does not disclose what etchants are used to etch the hardmask layer or the intermetal dielectric layer when it is comprised of organic material (col. 6, ln. 38-43). The admitted prior art discloses forming the via and line openings by etching the hardmask layer with a fluorocarbon based plasma and the organic intermetal dielectric layer is etched with an oxygen based plasma (pg. 3, ln. 30-pg. 4, ln. 4). At the time of the invention, it would have been obvious to one of ordinary skill in the art to etch the intermetal layer of Avanzino with an oxygen based plasma when the layer comprises an organic material as described by the admitted prior art while using a fluorocarbon based plasma to etch the inorganic hardmask layer of Avanzino as is also described by the admitted prior art because these etchants are well known for etching organic and inorganic layers, respectively.

4. Claims 7, 12 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art in view of Avanzino et al. (US 5,795,823) and Pellerin et al. as applied to claim 1 above and further in view of Huang et al. (US 5,635,423).

In reference to claims 7, 12 and 16, the admitted prior art discloses that the hardmask layer is inorganic but does not disclose what specific material it may be made of (pg. 3, ln. 9). Avanzino discloses that the hardmask layer comprises silicon nitride (col. 6, ln. 30-33). Huang discloses that an etch stop/hardmask layer may be made of such materials as silicon nitride or silicon oxynitride (col. 6, ln. 12-16). In fact, silicon nitride and silicon oxynitride are conventionally used in the art to comprise etch stop layers (as is also disclosed by Huang (col. 6, ln. 12-16)). At the time of the invention, it would have been obvious to one of ordinary skill in the art to form the hardmask layer of the admitted prior art from conventional etch stop materials such as silicon nitride or silicon oxynitride because these materials are well known etch stop materials.

4. Claims 28 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Avanzino et al. (US 5,795,823) in view of the admitted prior art as applied to claim 22 above, and further in view of Huang et al. (US 5,635,423).

In reference to claims 28 and 33, the admitted prior art discloses that the hardmask layer is inorganic but does not disclose what specific material it may be made of (pg. 3, ln. 9). Avanzino discloses that the hardmask layer comprises silicon nitride (col. 6, ln. 30-33). Huang discloses that an etch stop/hardmask layer may be made of such materials as silicon nitride or

silicon oxynitride (col. 6, ln. 12-16). In fact, silicon nitride and silicon oxynitride are conventionally used in the art to comprise etch stop layers (as is also disclosed by Huang (col. 6, ln. 12-16)). At the time of the invention, it would have been obvious to one of ordinary skill in the art to form the hardmask layer of the admitted prior art from conventional etch stop materials such as silicon nitride or silicon oxynitride because these materials are well known etch stop materials.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christy L. Novacek whose telephone number is (703) 308-5840. The examiner can normally be reached on Monday-Thursday and alternate Fridays 7:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on (703) 308-4940. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

CLN
August 13, 2001

Carl Whitehead Jr.

CARL WHITEHEAD, JR.
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800